

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

ATTY.'S DOCKET: NREL IR# 96-48



Applicant : Timothy A. Gessert)	Art Unit: Not Yet Accorded
)	
)	Examiner: Not Yet Accorded
)	
Filed: Not Yet Accorded)	
)	
Title: ION BEAM TREATMENT TO)	
PREPARE SURFACES OF PCdTe)	
FILMS)	

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 AND 1.98

Honorable Commissioner of
Patents and Trademarks
Box Patent Applications
Washington, D.C. 20231

Sir:

It is respectfully requested that the citations listed below be considered by the Patent and Trademark Office and be made of official record in the above-identified application.

In the opinion of the undersigned, the below-listed citations represent the closest art known to the undersigned during the preparation of the above-identified application. These citations may be material to the examination of the subject application and are therefore submitted in compliance with a duty of disclosure defined in 37 CFR §§ 1.56 and 1.97.

A concise explanation of the relevance of the pertinent listed patents are set forth below.

CONCISE EXPLANATION OF THE RELEVANCE OF
PERTINENT PATENTS & REFERENCES

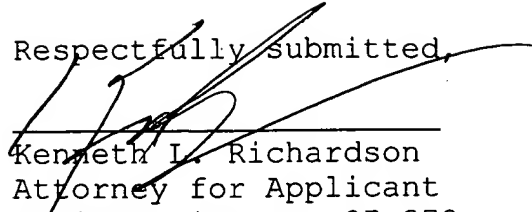
U.S. Patent 4,319,069 is deemed pertinent for its disclosure of chemical treatment of a p-CdTe surface prior to contacting to improve the contact characteristics, by utilizing an oxidizing agent and a leveling agent to form the Te layer.

U.S. Patent 4,456,630 is deemed pertinent in that it discloses a chemical treatment of a p-CdTe surface prior to contacting to improve contact characteristics, by use of an oxidizing acid plus a reducing agent.

U.S. Patent 4,766,084 is deemed pertinent for its disclosure of a process for producing an electric contact on a HgCdTe substrate having a p conductivity and application to the production of a N/P diode, and it specifically uses ion bombardment for removal etching of the SiO₂ insulator layer.

U.S. Patent 4,581,099 is deemed pertinent for its disclosure of a process for replacement of chemical etching with a process involving CF₄ plasma etching plus heat treatment to form an improved gate area in n-type α -Si on top of intrinsic α -Si.

Respectfully submitted,


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